PATENT SPECIFICATION

DRAWINGS ATTACHED

1,127,270

1,127,270

Inventors:—PETER ALAN EDWARD GARDNER, MICHAEL HENRY HALLETT and PETER JAMES TITMAN.

Date of Application and filing Complete Specification: 5 September, 1967. No. 40623/67.

Complete Specification Published: 18 September, 1968.

Index at Acceptance:—H3 T (1M3, 2B2, 2J, 2T3J, 2T4, 3X, 4C, 4EX, 4M, 4R, 5E); G4 C (1F, 2JX, 2K, 3F).

Int. Cl.:—H 03 K 15/18.

ERRATA

SPECIFICATION NO. 1,127,270

Page 1, line 26, *after* "second" *insert* "stable state and to generate the second"

Page 2, line 31, *for* "provided" *read* "providing".

Page 4, line 113, *for* "F" *read* "4"

Page 5, line 34, *for* "dull" *read* "null"

THE PATENT OFFICE,
23rd October 1968

D 109351/20

prising a transistor circuit having first and second stable states of conductivity and interrogable for first and second states respectively by different interrogation signals, the circuit being adapted on interrogation for the first stable state to generate a first output signal if the circuit is in the first stable state and to generate a second output signal if the circuit is in the second stable state, and being adapted on interrogation for the second stable state to generate the first output signal if the circuit is in the second output signal if the circuit is in the first stable state.

According to the invention, in a data storage cell, as hereinbefore defined, the transistor circuit has a third stable state of conductivity and is adapted to generate the first output signal when the circuit is in the third stable state in response to interrogation for the first stable state, and in response to interrogation for the second stable state.

The invention will be further explained by way of example with reference to the accompanying drawings, in which:—

FIGURE 1 is a schematic diagram of a typical known associative store;

FIGURE 2 is the truth table of a data storage cell used in an associative store of the kind illustrated in Figure 1;

atically, part of a known associative, or content-addressed store. The characterising feature of such a store is that a data word is retrieved from the store by specifying at least part of data contained in the word. This is in contrast to a conventional store in which a data word is retrieved by specifying the address in the store at which the word is located. For example, in an associative store in which each data word consists of a part number and the number of parts in stock, by specifying a part number the associated data word can be retrieved and the stock level found, or alternatively, by specifying a predetermined stock level, the part numbers of all those parts at that stock level can be found. In a conventional store, the latter information can only be found by accessing each data word and examining the stock level of each part.

The associative store 10 shown in Figure 1 includes an input register 11 comprising a plurality of binary data storage cells 12, a mask register 13 comprising a plurality of masking circuits 14, one circuit to each order of the input register 11, and a number of word stores 15 each comprising a plurality of data storage cells 16. When a word is entered into input register 11 all or part of the word is compared with the contents

SEE ERRATA SLIP ATTAC

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Int. Cl.:—H 03 K 15/18.

COMPLETE SPECIFICATION

Data storage cell

We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York, United States of America, of Armonk, New York 10504, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a data storage cell.

A data storage cell is defined as comprising a transistor circuit having first and second stable states of conductivity and interrogable for first and second states respectively by different interrogation signals, the circuit being adapted on interrogation for the first stable state to generate a first output signal if the circuit is in the first stable state and to generate a second output signal if the circuit is in the second stable state, and being adapted on interrogation for the second stable state to generate the first output signal if the circuit is in the second output signal if the circuit is in the first stable state.

According to the invention, in a data storage cell, as hereinbefore defined, the transistor circuit has a third stable state of conductivity and is adapted to generate the first output signal when the circuit is in the third stable state in response to interrogation for the first stable state, and in response to interrogation for the second stable state.

The invention will be further explained by way of example with reference to the accompanying drawings, in which:—

FIGURE 1 is a schematic diagram of a typical known associative store;

FIGURE 2 is the truth table of a data storage cell used in an associative store of the kind illustrated in Figure 1;

FIGURE 3 is the truth table of a data storage cell according to the invention;

FIGURE 4 is a circuit diagram of a data storage cell according to the invention;

FIGURE 5 is a circuit diagram of part of another data storage cell according to the invention;

FIGURE 6 is a modification of the data storage cell of Figure 5; and

FIGURE 7 is a tristable circuit comprising a data storage cell according to the invention.

Figure 1 of the drawings shows, schematically, part of a known associative, or content-addressed store. The characterising feature of such a store is that a data word is retrieved from the store by specifying at least part of data contained in the word. This is in contrast to a conventional store in which a data word is retrieved by specifying the address in the store, at which the word is located. For example, in an associative store in which each data word consists of a part number and the number of parts in stock, by specifying a part number the associated data word can be retrieved and the stock level found, or alternatively, by specifying a predetermined stock level, the part numbers of all those parts at that stock level can be found. In a conventional store, the latter information can only be found by accessing each data word and examining the stock level of each part.

The associative store 10 shown in Figure 1 includes an input register 11 comprising a plurality of binary data storage cells 12, a mask register 13 comprising a plurality of masking circuits 14, one circuit to each order of the input register 11, and a number of word stores 15 each comprising a plurality of data storage cells 16. When a word is entered into input register 11 all or part of the word is compared with the contents

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of each of the word stores 15. If the data being compared is identical with the contents of a word store 15 an indication to this effect is given at a match terminal 17 associated with the word store. An indication of lack of identity is given at a no match terminal 18. The comparison operation is illustrated schematically as a current switching operation under the control of current switches 20 of which there is one to each storage cell 16 of each word store. Current is supplied to a terminal 19. If the binary digit stored in the storage cell is equal to the digit with which it is being compared the switch 20 of the cell directs the current towards the match terminal 17. If the digits are unequal, switch 20 diverts the current towards the no match terminal 18. The data to be compared is supplied from the input register 11 as a marking of one out of the two lines 21 from each cell 12 of register 11. The lines 21 are connected to the cell 16 in each word store 15 in the associative store 10 which corresponds in order to the cell 12 from which the lines issue. The function of the masking register 13 is to mask from the word stores 15 the data in register 11 which is not to be compared with the contents of the word stores. Accordingly, masking register 13 is shown schematically as provided a switch 14 in each line 21 issuing from input register 11. When a switch 14 is open (as shown) the signal on connected line 21 does not reach the word stores 15. Each current switch 20 is arranged to direct current towards the match terminal 17 in the absence of any input signals on lines 21 connected to the cell 16 containing the switch. Such an input on lines 21 is known as a null input and is often in the form of balanced signals on both lines 21. Further details of the associative store 10 are not of relevance to the invention, but it will be understood that means are provided to utilize the signals on the match or no-match terminals to control the accessing of particular word stores.

From the above description, it will be understood that the data storage cell used in known associative stores has the truth table shown in Figure 2. The extreme left-hand column of the table shows the binary digit represented by state of the storage cell, while the top row represents the interrogating signals supplied to the cell on lines 21. The entries in the table show the response of the current switch 20 of the cell to the interrogating signal.

One of the drawbacks of the conventional associative store is that every state of every cell in the word stores would be significant without the masking register. If it required to ignore for comparison purposes the contents of a particular cell, it is necessary to operate the masking register which prevents comparison of all cells in the same column of the associative store as the particular cell. This consideration and a need for greater flexibility in the use of associative stores has led to the conclusion that it is desirable to provide a storage cell having the truth table shown in Figure 3. Each storage cell has three states represented by 1, 0 and X. When the storage cell is in the X state, it gives a match output to any interrogation signal.

According to the invention there is provided a transistor circuit for implementing a storage cell having 1, 0, and X states.

One example of a transistor circuit according to the invention is shown in Figure 4. The cell shown in Figure 4 has, in fact, four states. The fourth state, Y, is such that, in response to 1 or 0 interrogation signals, the cell issues a no match output. However, the provision and use of the fourth state is not an essential feature of the invention.

The data storage cell of Figure 4 comprises two bistable circuits each including a pair of directly cross-coupled transistors. The states of the cell are each characterised by two transistors being conductive, one from each pair. One bistable circuit comprises a double-emitter transistor T1 which is directly cross-coupled to transistor T2. A direct coupling is to be understood as a coupling which does not include a series impedance. The collector of transistor T1 is connected to a collector voltage supply line 41 through series resistors R1 and R3. The collector of transistor T2 is connected to line 41 through series resistors R2 and R3. The emitter of transistor T2 is directly connected to a reference voltage source 42, which is shown as ground. In practice the value of the reference voltage will depend on the characteristics of the circuit. Any voltage mentioned in this description is measured relative to the reference voltage. Emitter E11 of transistor T1 is directly connected to a word emitter line 43, the function of which is to provide match or no match signals. Emitter E12 of transistor T1 is directly connected to 0 bit line 44, the functions of which will be explained later. The other bistable circuit is comprised of transistor T3 and double-emitter transistor T4 which are directly cross-coupled in the same way as transistors T1 and T2. The collectors of transistors T3 and T4 are connected to collector voltage line 41 through a resistor network R4 to R6, identical with network R1 to R3. The emitter of transistor T3 is directly connected to the reference voltage ground 42 while emitter E41 of transistor T4 is directly connected to word emitter line 43 and emitter E42 of transistor T4 is directly connected to a 1 bit line 45, the functions of which will

be described later. Various switches have been schematically indicated in Figure 4 as mechanical switches having moving contact arms. In practice, these switches which are for supplying control voltages to the cell, would be embodied as electronic switches.

Switches 46 to 49 are three terminal switches. Switches 46 and 47 connect the 0 bit line 44 and the 1 bit line 45 respectively to voltages of −0.2V, 0V (the reference voltage), or +0.1V depending on the terminal on which the switch arm is closed. Switch 49, similarly, selectively connects the word emitter line 43 to voltages of −0.2V, 0V or +0.1V. Switch 48 terminals connect the collector voltage line to voltages of 3.0V or 2.0V, or render the line floating.

The four states of the data storage cell of Figure 4 are:

1 state: T2 and T4 conductive;
0 state: T1 and T3 conductive;
X state: T2 and T3 conductive; and
Y state: T1 and T4 conductive.

A no match condition is signalled by the presence of current on word emitter line 43 The 0 and 1 bit lines are used to set the data cell to a required state, to read the state of the data cell, and to supply interrogation signals which result in match or no match signals on line 43 according to the truth table of Figure 3 and a no match signal, in response to 1 or 0 interrogation signals, if the cell is in the Y state.

In the quiescent state, switch 48 is closed on the 3.0V terminal, and switches 46, 47 and 49 are closed on their respective 0V terminals.

In order to interrogate the cell for a match or no match output, and without changing the state of the data cell, switches 46 and 47 are manipulated. If the interrogation is for the 0 state, switch 46 is closed on the −0.2V terminal and switch 47 is closed on the +0.1V terminal. If the cell is in the 0 state, transistor T1 is conducting and the reduction of voltage on line 44 causes substantially all the current to flow only in emitter E12 and line 44, substantially none reaching the word emitter line 43. Transistor T4 is not conducting and the change in voltage on line 45 does not affect this transistor, with the result that no current reaches line 43 from transistor T4. Since there is substantially no current on line 43, a match is indicated. If the cell is in the 1 state, transistor T4 is conducting. No current reaches line 43 from transistor T1, but the raised voltage on line 45, without affecting the conductive state of transistor T4, ensures that current flows in emitter E41 and line 43 producing a no match signal. If the cell is in the X state, neither transistor T1 nor transistor T4 is conducting and no current will reach line 43, indicating a match. If the cell is in the Y state transistor T4 is conducting and current is steered onto line 43, indicating a no match. To interrogate for the 1 state, switch 47 is closed on the −0.2V terminal and switch 46 is closed on the +0.1V terminal. In similar fashion to the 0 state interrogation just described, current is diverted to the word emitter line 43 if the cell is in the 0 or Y states, but no current reaches the line 43 if the cell is in the 1 or X states. For a null interrogation both switches 46 and 47 are closed on the −0.2V terminal thus preventing current reaching the line 43 whatever the state of the cell.

In order to read the state of the cell, without changing that state, switch 49 is closed on the +0.1V terminal and switches 46 and 47 are closed on their 0V terminals. Current is then diverted onto neither, both or one of the bit lines 44 and 45, depending on the state of the cell. If transistor T1 is conductive, current flows through emitter E12 and line 44, while if transistor T4 is conductive current flows through emitter E42 and line 45. Thus, current in only line 44 indicates that the cell is in the 0 state, current in only line 45 indicates that the cell is in the 1 state, current in neither line 44 nor 45 indicates that the cell is in the X state and current in both lines 44 and 45 indicates that the cell is in the Y state.

Writing into the cell of Figure 4 is effected by closing switch 48 on the 2.0V terminal and closing switch 49 on the 0.1V terminal, thereby lowering the switching threshold of the bistable circuits, and operating switches 46 and 47 to apply appropriate voltages on the bit lines. Since the switching threshold has thereby been lowered, the same voltages as are used in interrogating the cell are now effective to switch the bistable circuits. If it is required that transistor T1 be made conducting, switch 46 is closed on the −0.2V terminal, or if transistor T1 is to be made non-conducting switch 46 is closed on the +0.1V terminal. Similarly, switch 47 is closed on the −0.2V or +0.1V terminal, respectively, if transistor T4 is to be made conducting or non-conducting, respectively. Writing may be effected without changing the previous state of the cell. Thus, if transistors T1 and T3 are conducting and it is required to cause the cell to assume the X state, this may be done by closing switch 48 on the 2.0V terminal, switch 49 on the +0.1V terminal, and switch 46 on the +0.1V terminal, thereby sending transistor T1 non-conducting and transistor T2 conducting. Alternatively, writing may be effected after destroying the previous state of the cell by momentarily closing switch 48 on the floating terminal.

As shown, switch 49 has a −0.2V terminal. This is used to isolate the data cell from the bit lines, since, if the switch is

closed in this terminal signals on a bit line are effective to commute current between the emitters of the connected double-emitter transistor, or to change the conductive state of the resistor. Such isolation is necessary when it is required to read, or write into, a data cell connected to the same bit lines as those shown in Figure 4.

In order to prevent spurious currents it is necessary that the transistors be operated out of hard saturation. This leads to difficulties in tolerancing the signals on the bit lines, for it is necessary that the signals on the bit lines be sufficient to switch current between the emitters of the two-emitter transistors without disturbing the state of the cell. One method of achieving higher switching thresholds while keeping the transistors out of saturation is illustrated in Figure 5 which shows only one bistable circuit of a cell according to the invention. Elements common to Figures 4 and 5 are referenced as in Figure 4. Emitter follower circuits T5 and R7 and T6 and R8 are connected in the collector to base cross-connections of the bistable circuit. The effect of the emitter followers is to necessitate higher magnitude voltages on bit line 44 in order to switch the bistable circuit than would be the case, with the same voltage on line 41, without the emitter followers. Emitter followers are also provided in the cross-coupling of the transistors of the other bistable circuit (not shown) of the data cell.

Figure 6 shows a modification of the circuit of Figure 5. For clarity, both bistable circuits comprising the data cell have been shown in Figure 6. The switch 48 in the collector voltage line is dispensed with and is replaced by a switch 61, the contact arm of which is movable between terminals supplying 0V and a negative voltage respectively, and is connected to the ends, which are commoned, of the emitter resistors, such as R7, R8, remote from the emitter follower transistors, such as T5 and T6. The collectors of the emitter follower transistors T5, T6, of the bistable circuit including transistors T1 and T2 are commoned and connected between series-connected resistors R3*a*, R3*b* which replace the resistor R3 of Figures 4 and 5. The collectors of the emitter follower transistors of the other bistable circuit comprising the data cell are similarly connected between resistors R6*a*, R6*b* which replace resistors R6.

The circuit of Figure 6 provides an effective means for selectively varying the switching thresholds of the bistable circuits so that signals on the bit lines 44, 45 may be used either to interrogate the state of the data cell or to write new information into the cell. When the contact arm of switch 61 is closed on the 0V terminal interrogation signals of predetermined voltages are effective to commute current between the emitters of the double-emitter transistors T1, T4 but do not switch the bistable circuits. Under these conditions the emitter followers operate with very little power dissipation. By closing switch 61 on the negative terminal, the currents through resistors R3*b* and R6*a* are reduced and the currents through the emitter resistors increased. This renders the bistable circuits much more sensitive to the signals on bit lines 44 and 45, and signals of the same predetermined voltages as the interrogation signals are effective to switch the bistable circuits.

Figure 7 shows a tristable circuit suitable for use as a data cell according to the invention. The cell comprises double-emitter transistors T7, T8 and a conventional transistor T9. The collectors of transistors T8 and T9 are coupled to the base of transistor T7 through the resistors R9, R10, respectively, and the emitter follower circuit comprising transistor T10 and resistor R11. The collectors of transistors T9 and T7 are coupled to the base of transistor T8 through resistors R12, R13, respectively, and the emitter follower circuit comprising transistor T11 and resistor R14. The collectors of transistors T7 and T8 are coupled to the base of transistor T9 through resistors R15, R16, respectively, and the emitter follower circuit comprising transistor T12 and resistor R17. Emitter E71 of double emitter transistor T7 is directly connected to bit 0 line 71 and emitter E81 of double-emitter transistor T8 is directly connected to bit 1 line 72. Emitter E72 of transistor T7 and emitter E82 of transistor T8 are directly connected to word emitter line 73. The methods of interrogating the state of the data cell of Figure 7 and of reading, or writing into, the cell are similar to those described with reference to Figure 4 and involve selectively connecting the bit and word emitter lines 71 to 73 to different voltage sources. The means for effecting such connections may comprise switches such as are shown in Figure F and which have, for clarity, been omitted from Figure 7.

The data cell of Figure 7 has three stable states each characterized by one out of the three transistors being conductive. The 0 state is characterized by transistor T7 being conductive, the 1 state by transistor T8 being conductive, and the X state by transistor T9 being conductive. The circuit of Figure 7 effectively comprises three threshold circuits which are, respectively, resistors R9, R10 and transistor T7, resistors R12, R13 and transistor T8, and resistors R15, R16 and transistor T9. The emitter followers connected between the resistors and the base of the transistor associated with the resistors are provided, as in the embodiments of Figures 5 and 6, to raise the d.c. level at the

base, thereby preventing saturation of transistors T7, T8, T9 of the transistor. The provision of the emitter followers is not essential but is a desirable feature of the design. Each threshold circuit is such that if and only if both the transistors, for example, T8 and T9, the collectors of which are directly connected to the resistors, for example R9, R10, are non-conductive is the voltage at the base of the transistor, for example T7, to which the resistors are connected appropriate to maintain the latter transistor conducting. It follows that only one of the transistors T7 to T9 is conductive at a time, and that transistor T9 can selectively be rendered conducting or nonconducting by controlling the conductivity of transistors T7 and T8 by suitable voltages applied on the bit lines 71, 72, and the word emitter line 73.

Interrogation for 0 is effected, as for the cell of Figure 4, by placing such voltages on the bit lines 71, 72, that if current is flowing in transistor T7 it is steered through emitter E71 to the 0 bit line, whereas if current is flowing in transistor T8 it is steered through emitter E82 to the word emitter line 73, thereby indicating no match. Interrogation for 1 is similar, with voltages on the bit lines reversed. If, upon either interrogation, the circuit is in the X state with T9 conductive, no significant current can reach the word emitter line 73 and a match is signalled. A dull interrogation is effected by placing such voltages on the bit lines that no significant current can reach the word emitter line even if T7 or T8 is conductive. Reading is effected by placing such a voltage on word emitter line 73 that if current is flowing in transistor T7 or T8 it is diverted to the associated bit line 71 or 72 thereby indicating the state of the cell. If T9 is conductive, no current will appear on either bit line. Writing is effected by placing such a voltage on the word emitter line 73 that the switching threshold of transistors T7 and T8 is lowered, while placing voltages on the bit lines such as to send the required transistor conductive or nonconductive.

The circuits described with reference to Figures 4 to 7 are particularly suitable for embodiment as integrated circuits.

WHAT WE CLAIM IS:—

1. A data storage cell, as hereinbefore defined, wherein the transistor circuit has a third stable state of conductivity and is adapted to generate the first output signal when the circuit is in the third stable state in response to interrogation for the first stable state, and in response to interrogation for the second stable state.

2. A data storage cell as claimed in claim 1, wherein the transistor circuit is adapted, whatever the stable state of the circuit, to generate the first output signal in response to a predetermined interrogation signal, different from the signals used in interrogation for the first or second stable states.

3. A data storage cell as claimed in any one of the preceding claims, including two control lines and an output line, wherein interrogation signals are applied on the control lines, resulting in a first or second output signal on the output line.

4. A data storage cell as claimed in claim 3, wherein a read signal applied on the output line results in signals on the control lines which are indicative of the stable state of conductivity of the circuit.

5. A data storage cell as claimed in claim 3 or claim 4, in which the transistor circuit includes two double-emitter transistors, one emitter of each transistor being connected to the output line and the other emitters being connected each to a different control line.

6. A data storage cell as claimed in claim 5, in which the transistor circuit comprises two bistable circuits, each comprising a transistor and a double-emitter transistor, the stable states of conductivity of the transistor circuit each being defined by a different two transistors being conductive, one conductive transistor being from each bistable circuit.

7. A data storage cell as claimed in claim 6, wherein the bases and collectors of the transistors comprising a bistable circuit are directly cross coupled.

8. A data storage cell as claimed in claim 6, wherein the bases and collectors of the transistors comprising a bistable circuit are cross coupled, each coupling including a respective emitter follower circuit.

9. A data storage cell as claimed in any one of the preceding claims, wherein the transistor circuit has a fourth stable state of conductivity and is adapted to generate the second output signal when the circuit is in the fourth stable state in response to interrogation for the first stable state, and in response to interrogation for the second stable state.

10. A data storage cell as claimed in claim 6, wherein the transistor circuit is a tristable circuit comprising a transistor and two double-emitter transistors, each stable state of the circuit being defined by a different one of the transistors being conductive.

11. A data storage cell substantially as described with reference to Figure 4 of the accompanying drawings.

12. A data storage cell substantially as described with reference to Figure 5 of the accompanying drawings.

13. A data storage cell substantially as described with reference to Figure 6 of the accompanying drawings.

14. A data storage cell substantially as described with reference to Figure 7 of the accompanying drawings.

J. D. LANCASTER,
Chartered Patent Agent,
Agent for the Applicants.

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Published at the Patent Office, 25 Southampton Buildings, London, W.C.2. from which copies may be obtained.

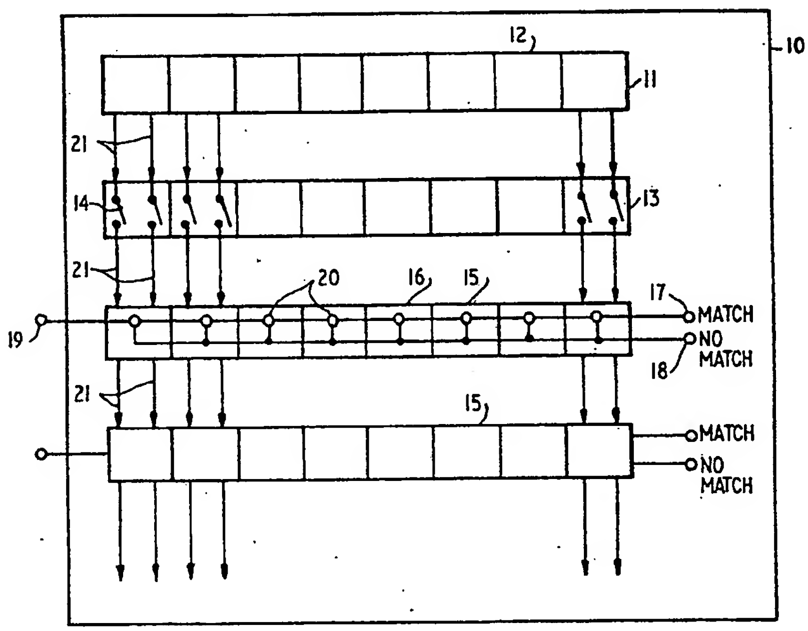


FIG. 1

INPUT

STORED	0	1	NULL
0	M	N	M
1	N	M	M

M=MATCH
N=NO MATCH

FIG. 2

INPUT

STORED	0	1	NULL
0	M	N	M
1	N	M	M
X	M	M	M

M=MATCH
N=NO MATCH

FIG. 3

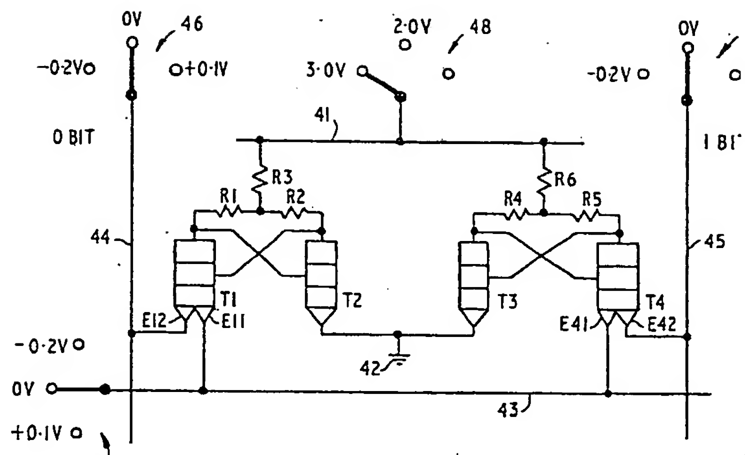

0V
46
2·0V
48
0V
−0·2V
+0·1V
3·0V
−0·2V
0 BIT
41
I BI
R3
R6
R1
R2
R4
R5
44
45
T1
T2
T3
T4
E12
E11
E41
E42
−0·2V
42
0V
43
+0·1V
49

FIG. 4

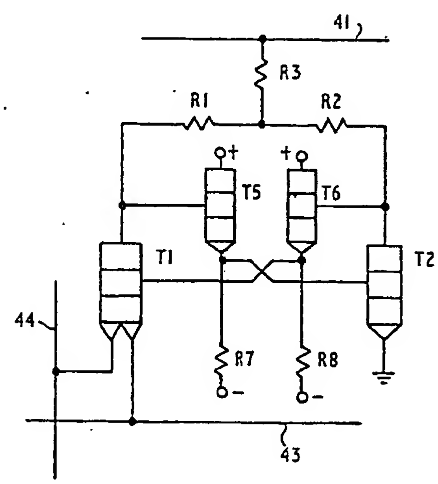
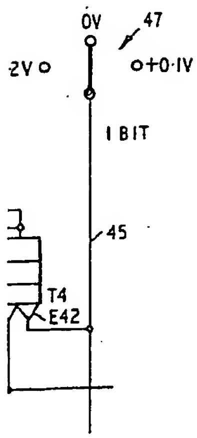

41
R3
R1
R2
+
+
T5
T6
T1
T2
44
R7
R8
−
−
43

FIG. 5

1,127,270 COMPLETE SPECIFICATION
3 SHEETS *This drawing is a reproduction of the Original on a reduced scale.*
SHEETS 2 & 3



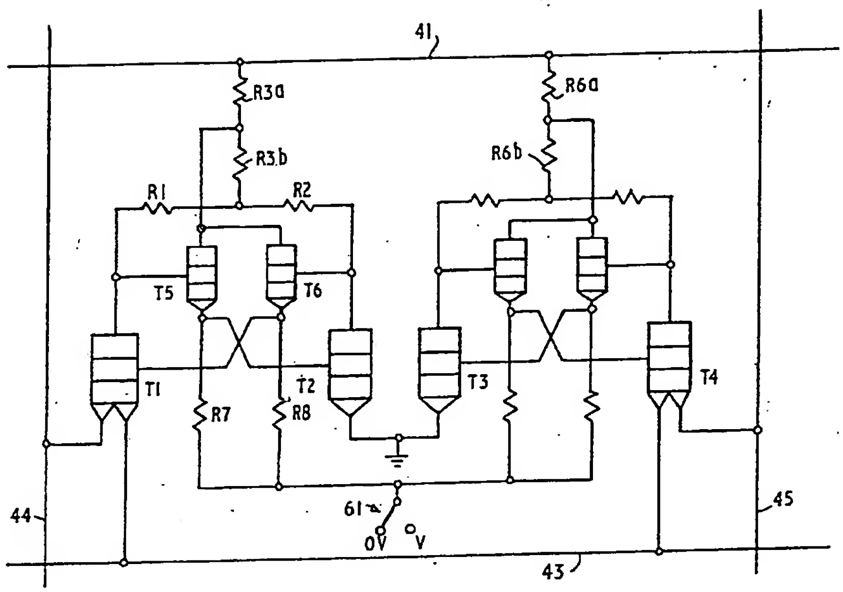


FIG. 6

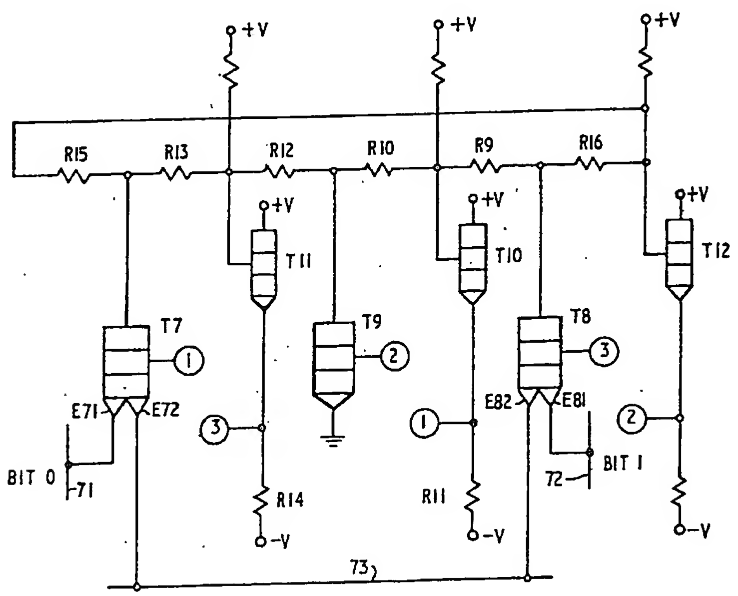


FIG 7

1,127,270 COMPLETE SPECIFICATION
3 SHEETS
This drawing is a reproduction of the Original on a reduced scale.
SHEETS 2 & 3

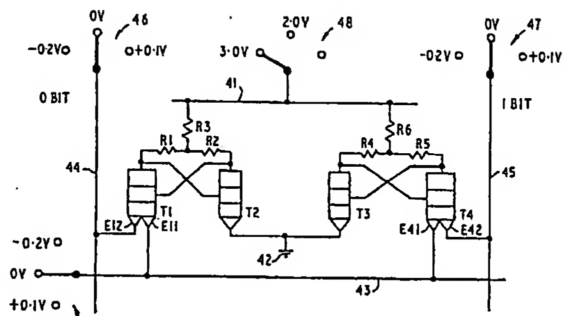


FIG. 4

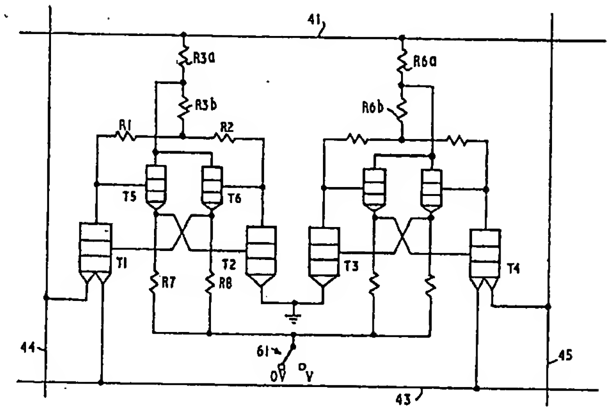


FIG. 6

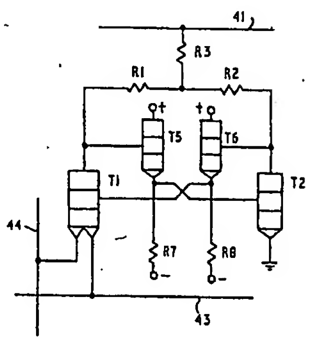


FIG. 5

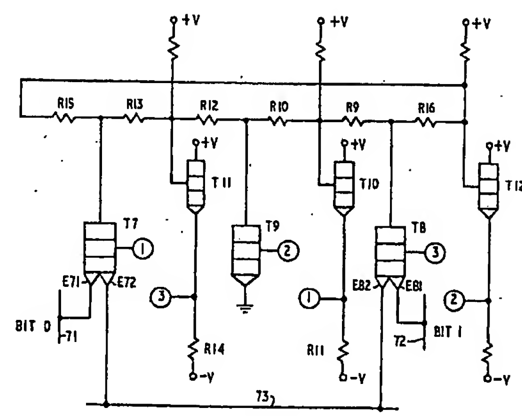


FIG. 7